Product Preview **Buffer**

The MC74VHC1G50 is an advanced high speed CMOS buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffered output which provides high noise immunity and stable output.

The MC74VHC1G50 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1G50 to be used to interface 5V circuits to 3V circuits.

- High Speed: $tp_D = 3.5ns$ (Typ) at $V_{CC} = 5V$
- Low Power Dissipation: $I_{CC} = 2\mu A$ (Max) at $T_A = 25^{\circ}C$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 1500V; MM > 200V

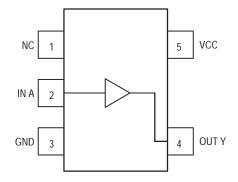
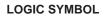


Figure 1. 5-Lead SOT-353 Pinout (Top View)







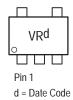
ON Semiconductor

Formerly a Division of Motorola http://onsemi.com



SC-88A / SOT-353 DF SUFFIX CASE 419A

MARKING DIAGRAM



	PIN ASSIGNMENT								
1	NC								
2	IN A								
3	GND								
4	OUT Y								
5	VCC								

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

FUNCTION TABLE

Y Output
L
Н
•

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS*

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V _{CC}	-0.5 to +7.0	V
DC Input Voltage	VIN	-0.5 to +7.0	V
DC Output Voltage V _{CC} = 0 High or Low State	Vout	−0.5 to 7.0 −0.5 to V _{CC} + 0.5	V
Input Diode Current	Iк	-20	mA
Output Diode Current $(V_{OUT} < GND; V_{OUT} > V_{CC})$	IOK	+20	mA
DC Output Current, per Pin	IOUT	+25	mA
DC Supply Current, V_{CC} and GND	ICC	+50	mA
Power dissipation in still air, SC–88A †	PD	200	mW
Lead temperature, 1 mm from case for 10 s	ΤL	260	°C
Storage temperature	T _{stg}	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SC-88A Package: -3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	VCC	2.0	5.5	V
DC Input Voltage	VIN	0.0	5.5	V
DC Output Voltage	VOUT	0.0	VCC	V
Operating Temperature Range	TA	-55	+85	°C
Input Rise and Fall Time $$V_{CC}$=3.3V\pm0.3V$\\ V_{CC}=5.0V\pm0.5V$$	t _r ,t _f	0 0	100 20	ns/V

			Vcc	т	A = 25°0	C	T _A ≤	85°C	TA ≤ '	125°C	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Мах	Min	Мах	Min	Max	Unit
VIH	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
VIL	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
VOH	Minimum High–Level Output Voltage V _{IN} = V _{IH} or V _{IL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V _{OL}	Maximum Low–Level Output Voltage VIN = VIH or VIL	VIN = VIH or VIL IOL = 50µA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μΑ
ICC	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA

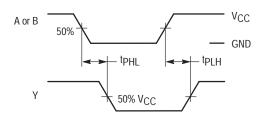
DC ELECTRICAL CHARACTERISTICS

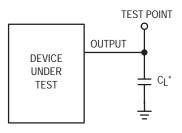
AC ELECTRICAL CHARACTERISTICS ($C_{load} = 50 \text{ pF}$, Input $t_r = t_f = 3.0 \text{ns}$)

				Г	F _A = 25°0	C	T _A ≤	85°C	TA ≤ ′	125°C	
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Maximum Propogation Delay,	$V_{CC} = 3.0 \pm 0.3 V$	C _L = 15 pF C _L = 50 pF		4.5 6.4	7.1 10.6		8.5 12.0		10.0 14.5	ns
	Input A to Y	$V_{CC} = 5.0 \pm 0.5 V$	C _L = 15 pF C _L = 50 pF		3.5 4.5	5.5 7.5		6.5 8.5		8.0 10.0	
C _{IN}	Maximum Input Capacitance				4	10		10		10	pF
Typical @ 25°C, V _{CC} = 5.0V											
Срп	Power Dissipation Car	pacitance (Note 1.)						8.0			рF

 CPD
 Power Dissipation Capacitance (Note 1.)
 8.0
 pF

 1. CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: ICC(OPR)=CPD • VCC • fin + ICC. CPD is used to determine the no-load dynamic power consumption; PD = CPD • VCC² • fin + ICC • VCC.





*Includes all probe and jig capacitance

Figure 3. Test Circuit

Figure 2. Switching Waveforms

DEVICE ORDERING INFORMATION

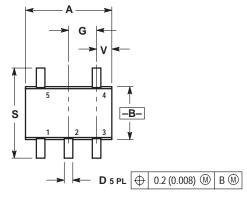
			Device Nome	nclature				
Device Order Number	Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape & Reel Suffix	Package Type	Tape and Reel Size
MC74VHC1G50DFT1	MC	74	VHC1G	50	DF	T1	SC-88A / SOT-353	7–Inch/3000 Unit

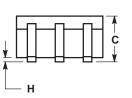
PACKAGE DIMENSIONS

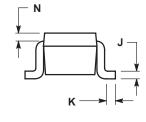
SC-88A / SOT-353 DF SUFFIX 5-LEAD PACKAGE CASE 419A-01 **ISSUE B**

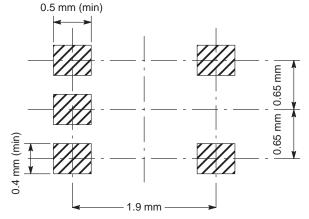
NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MM.

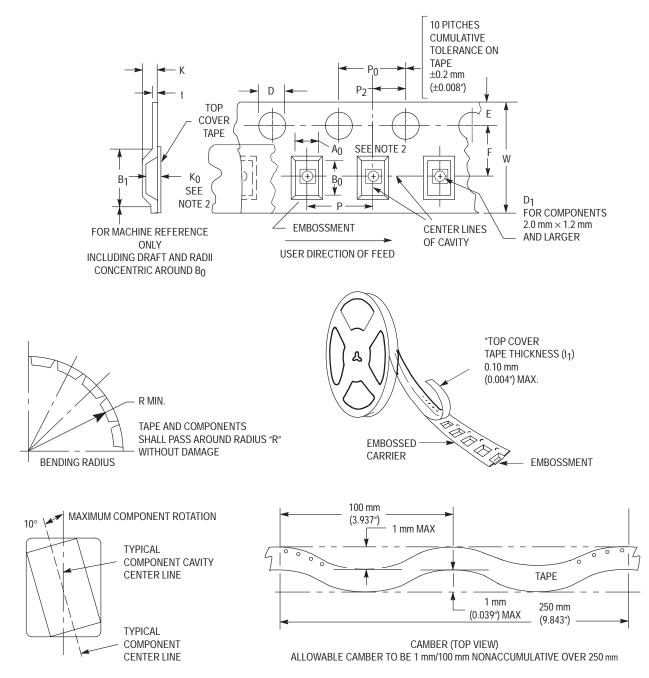
	INC	HES	MILLIM	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.071	0.087	1.80	2.20
В	0.045	0.053	1.15	1.35
С	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026	BSC	0.65	BSC
Н		0.004		0.10
J	0.004	0.010	0.10	0.25
К	0.004	0.012	0.10	0.30
Ν	0.008	REF	0.20	REF
S	0.079	0.087	2.00	2.20
٧	0.012	0.016	0.30	0.40













Tape Size	B ₁ Max	D	D ₁	E	F	к	Р	P ₀	P ₂	R	т	w
8 mm	4.35 mm (0.171")	1.5 +0.1/ -0.0 mm (0.059 +0.004/ -0.0")	1.0 mm Min (0.039″)	1.75 ±0.1 mm (0.069 ±0.004")	3.5 ±0.5 mm (1.38 ±0.002")	2.4 mm (0.094")	4.0 ±0.10 mm (0.157 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.1 mm (0.079 ±0.002")	25 mm (0.98")	0.3 ±0.05 mm (0.01 +0.0038/ -0.0002")	8.0 ±0.3 mm (0.315 ±0.012")

FMBOSSED	CARRIER	DIMENSIONS	(See Notes	1 a	and 2)
LINDOOOLD		DIMENSION	0000110100	1 0	$and \mathbf{z}_{j}$

1. Metric Dimensions Govern–English are in parentheses for reference only.

 A₀, B₀, and K₀ are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

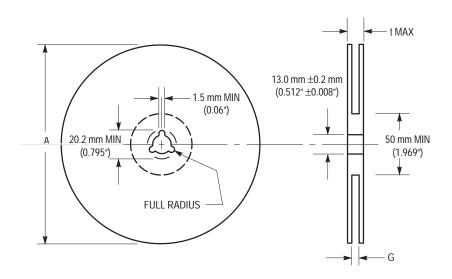
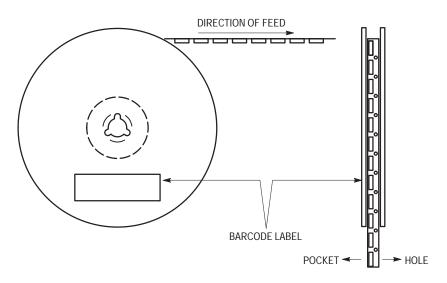


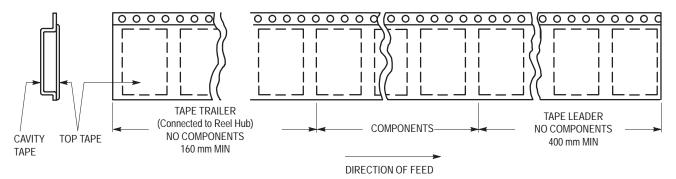
Figure 5. Reel Dimensions

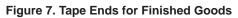
REEL DIMENSIONS

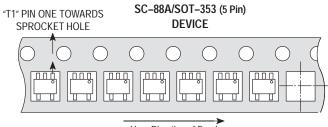
Tape Size	A Max	G	t Max
8 mm	330 mm	8.400 mm, +1.5 mm, -0.0	14.4 mm
	(13″)	(0.33", +0.059", -0.00)	(0.56″)











User Direction of Feed

Figure 8. Reel Configuration

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